Digital Logic Compared

Tackling compatibility issues

By David Daamen

In response to repeated requests, in this article we present an overview of a number of logic families and their properties. We also briefly examine certain important parameters. Finally, we explain what you need to pay attention to when working with digital logic.

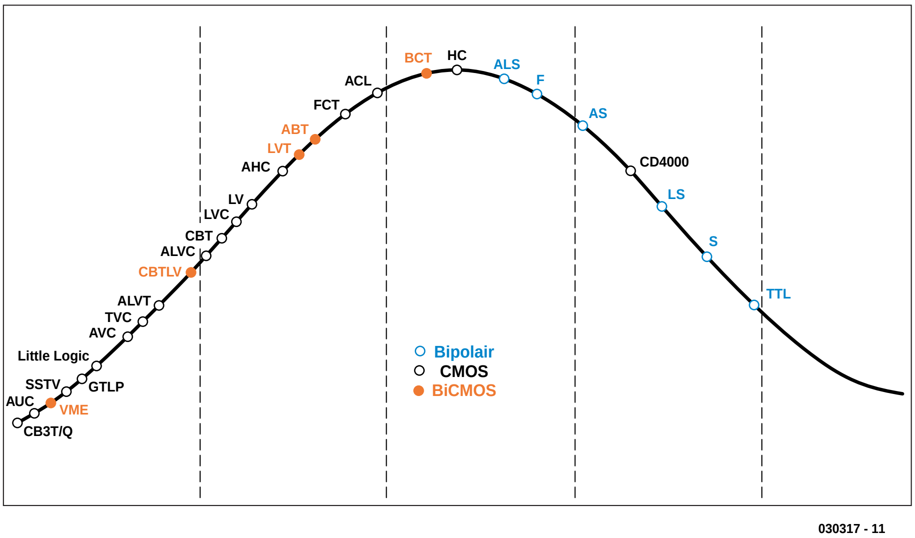


Figure 1. Market share of various logic families.

Although the ability of transistors to amplify signals excited the most interest from the very start, nowadays transistors are probably more often used as switches. It is precisely this (digital) application that forms the basis for this article, since a wide variety of logic functions can be implemented using combinations of switching transistors, thus enabling us to have transistors do our computations.

The importance of digital-logic building blocks can readily be seen from the history of the various 'logic families'. Many of them are already obsolete, and new ones are yet to come. This means that we certainly cannot deal with this entire subject within the scope of this article. To help give you a better idea of the present state of affairs, we direct your attention to **Figure 1**.

In this capsule summary of the current market share of the various families (*source:* Texas Instruments), the families that are being phased out are shown at the right. As you can see, it is thus not a good idea to use TTL (for example) in new designs. At the far left, you can see a number of families that are just now being introduced. These families are smaller and even faster, or they may have lower power consumption. Incidentally, the latter two properties — high speed and low power consumption — are usually mutually contradictory, as we will see later on.

In this article, we concentrate on the families that are presently the most interesting for electronics hobbyists. For instance, we do not give any attention to the fast emitter-coupled logic (ECL) family, due to its excessively high price by hobbyist standards.

What makes it tick

Among the older, still 'living' members of the collection of digital logic families, the previously mentioned TTL family is probably the best

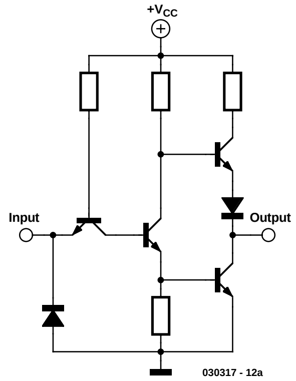


Figure 2a. A bipolar TTL inverter.

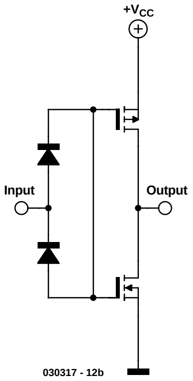


Figure 2b. A CMOS inverter.

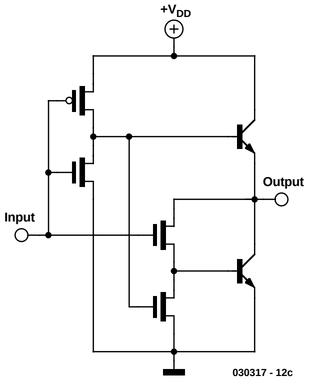


Figure 2c. A BiCMOS inverter.

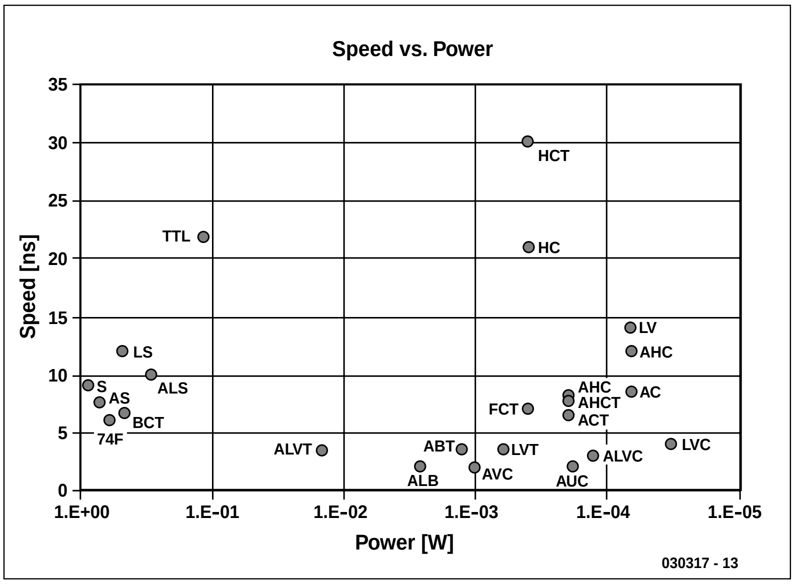


Figure 3. Speed versus power: a measure of performance.

known. A TTL IC is built using bipolar transistors. 'TTL' stands for 'transistor-transistor logic'. The structure of a simple gate using TTL technology, such as an inverter, is shown schematically in **Figure 2a**.

For comparison, **Figure 2b** shows the schematic of an inverter built with CMOS logic. CMOS ICs are constructed using n- and p-channel MOSFETs, which are complementary types of field-effect transistors. This is why they are called 'CMOS logic', since 'CMOS' stands for 'complementary metal oxide semiconductor'. Finally, **Figure 2c** shows the internal schematic diagram of a BiCMOS inverter. This type of inverter is built using a combination of bipolar and CMOS transistors.

ICs made with CMOS technology use much less power than their bipolar predecessors, since in principle a CMOS IC consumes power only when it switches states. However, CMOS ICs have the disadvantage that their FET inputs are much more vulnerable to damage from static electricity and excessive input currents in general.

Important parameters

For hobbyists, in many cases the availability and prices of the components to be used are the primary considerations in designing a circuit. As applications become more professional, speed and power consumption quickly become important factors in selecting specific components or families of components. The 'speed–power product' is frequently used to compare the performance of different logic series. This product is shown graphically in **Figure 3** for a number of well-known families.

This chart is based on typical values of power consumption and speed for each of the families. In this case, the speed refers to the typical time it takes for a change at the input to affect the state of the output. This can be illustrated by the diagram in **Figure 4**, which shows that the time delay (propagation delay) for the associated AND gate is 3 ns. The output does not go high until three nanoseconds after the input goes high. The same applies to the high-to-low transition.

Another important parameter is the noise margin. This number expresses the difference in the voltage levels of the driver and the receiver for a particular logic value. We can thus calculate the noise margin for logic 0 and logic 1 as follows:

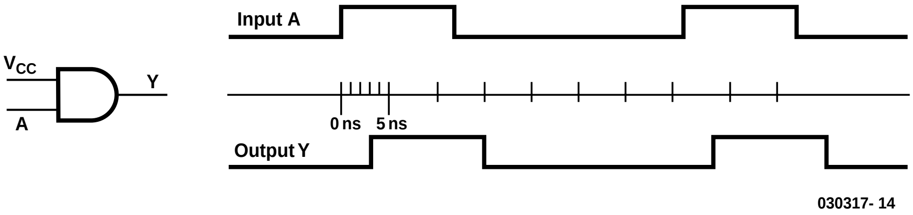
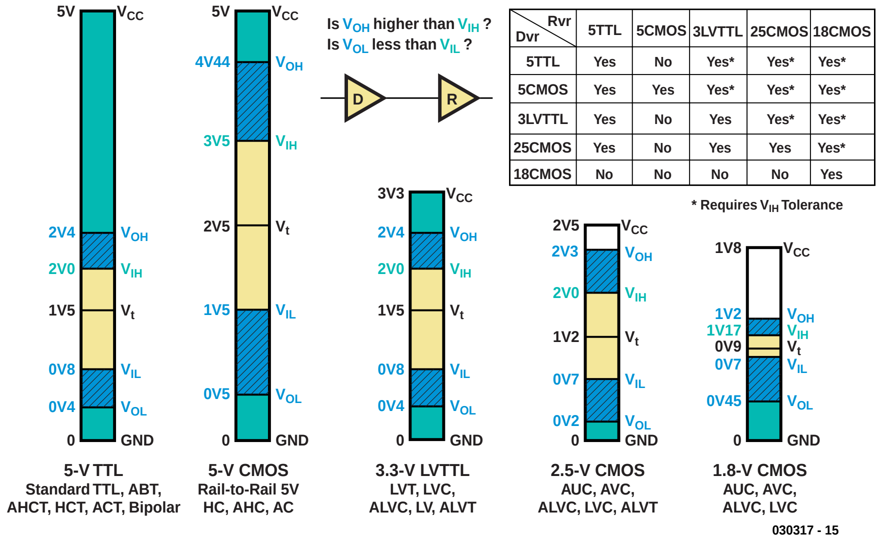


Figure 4. Propagation delay diagram for a CMOS AND gate.



Rvr Dvr	5TTL	5CMOS	3LVTTL	25CMOS	18CMOS
5TTL	Yes	No	Yes*	Yes*	Yes*
5CMOS	Yes	Yes	Yes*	Yes*	Yes*
3LVTTL	Yes	No	Yes	Yes*	Yes*
25CMOS	Yes	No	Yes	Yes	Yes*
18CMOS	No	No	No	No	Yes

* Requires V_{IH} Tolerance

Figure 5. Input and output levels. (Note: when calculating noise margins and compatibility, use the minimum values for 'Output High' and the maximum values for 'Output Low'. A compatibility marked with * in the table is only true for ICs that can tolerate a high input voltage, which is referred to as 'V_{ih} tolerance'. Refer to the data sheets of specific ICs.)

Table I. Overview of a number of families.

		Compatibility		Drive		Static Current	Speed
		Input	Output	I_{ol}	I_{oh}	I_{cc}	$T_{pd\ max}$
Family	**Technology**	V_{il}/V_{ih}	V_{ol}/V_{oh}	(mA)	(mA)	(mA)	(ns)
1.8 V							
AUC	CMOS	*CMOS*	*CMOS*	8	–8	0.01	2
2.5 V							
AVC	CMOS	*CMOS*	*CMOS*	8	–8	0.04	2
3.3 V							
ALVT	BiCMOS	*CMOS*	*LVTTL*	24	–8	4.5	3.5
LVT	BiCMOS	*LVTTL*	*LVTTL*	64	–32	0.19	3.5
ALVC	CMOS	*LVTTL*	*LVTTL*	24	–24	0.04	3
LVC	CMOS	*LVTTL*	*LVTTL*	24	–24	0.01	4
ALB	BiCMOS	*LVTTL*	*LVTTL*	25	–25	0.8	2
AC	CMOS	*CMOS*	*CMOS*	12	–12	0.02	8.5
AHC	CMOS	*CMOS*	*CMOS*	4	–4	0.02	11.9
LV	CMOS	*LVTTL*	*LVTTL*	8	–8	0.02	14
5 V							
FCT	BiCMOS	*TTL*	*TTL*	64	–15	0.08	7
ABT	BiCMOS	*TTL*	*TTL*	64	–32	0.25	3.5
AHC	CMOS	*CMOS*	*CMOS*	8	–8	0.04	7.5
AHCT	CMOS	*TTL*	*CMOS*	8	–8	0.04	7.7
AC	CMOS	*CMOS*	*CMOS*	24	–24	0.04	6.5
ACT	CMOS	*TTL*	*CMOS*	24	–24	0.04	8
74F	Bipolar	*TTL*	*TTL*	64	–15	120	6
BCT	BiCMOS	*TTL*	*TTL*	64	–15	90	6.6
HC	CMOS	*CMOS*	*CMOS*	6	–6	0.08	21
HCT	CMOS	*TTL*	*CMOS*	6	–6	0.08	30
AS	Bipolar	*TTL*	*TTL*	64	–15	143	7.5
ALS	Bipolar	*TTL*	*TTL*	24	–15	58	10
LS	Bipolar	*TTL*	*TTL*	24	–15	95	12
S	Bipolar	*TTL*	*TTL*	64	–15	180	9
TTL	Bipolar	*TTL*	*TTL*	16	–0.4	22	22

Noise Margin Output High =
V_{OH} *[driving device]* – V_{IH} *[receiving device]*

Noise Margin Output Low =
V_{IL} *[receiving device]* – V_{OL} *[driving device]*

To calculate the noise margin for a logic 1, we thus take the voltage level of the driving gate for a high output (V_{OH}) and subtract the voltage level for which the receiving gate detects a logic 1 (V_{IH}). For a low level, the same procedure applies, but we use the values V_{IL} and V_{OL} instead.

The noise margin can also be used for other purposes than assessing the 'noise immunity' (for which higher values are better). It can be used to check whether certain families are compatible with regard to signal levels. A negative value for the noise margin is a sign of incompatibility!

The final important set of parameters that we want to examine here are the fan-in and fan-out. These numbers indicate how many gates a given gate can drive, and they are determined by the currents supplied and drawn by the gates.

Fan-out Output High =
I_{OH} *[driving device]* / I_{IH} *[receiving device]*

Fan-out Output Low =
I_{OL} *[driving device]* / I_{IL} *[receiving device]*

As you can see, these calculations must again be made for each of the two logic levels. Naturally, the smaller of the resulting numbers determines the actual fan-out. The fan-out calculations can be used not only for the gates of a particular family, but also among different families.

Overview

Now that we have identified the most important parameters, it's time to present an overview. **Table 1** shows the supply voltages and the technologies used for a number of families, along with the logic level values under the 'Compatibility' heading. These values are further elaborated in **Figure 5**. Note that the indicated values are only representative. When making the calculations, it is best to use values taken from the data sheet for a particular component. This also applies to the values listed for drive current and static current in Table 1. Like the delay time *Tpd(max)*, the listed values are average or typical values for a family.

Using digital logic

When you actually use digital logic, there are a number of things you have to keep in mind. First, you have to watch out for possible incompatibilities among various versions made by different manufacturers. Each type of IC has a unique name, which can always be used to find a data sheet for it (on the Internet). Unfortunately, space limitations prevent us from describing all the possible options, but the naming convention for Texas Instruments ICs is shown in **Figure 6** as an example.

Naturally, you must also take maximum input currents into account in your design. Inputs should be protected against voltage spikes, such as may originate from electrostatic discharge (ESD). One way to do this is to connect a pair of reverse-biased diodes between the input and the supply voltage and the input and ground. These diodes will divert voltage spikes, thus protecting the input. Special transient protection diodes are commercially available, and there are also complete ICs based on the same principle, which can be used for applications such as protecting a complete bus with a single IC. By the way, most families can tolerate being touched by a person charged to 24 V; under normal circumstances, this provides adequate protection.

The next consideration is that connections between ICs, and between ICs and the 'outside world', must be kept as short as possible. As the operating speed increases, it quickly becomes necessary to regard long interconnecting lines as transmission lines. Phenomena such as reflections and overshoots can be controlled by using termination resistors. It is also better to avoid long parallel traces on circuit boards,

Table2. Summary list of manufacturers.

	T I	Fairchild	Hitachi	IDT	ON	Pericom	Philips	Toshiba
Bipolar	ALS	ALS	–	–	–	–	ALS	–
	AS	AS	–	–	–	–	–	–
	74F	F	–	–	F	–	F	–
	LS	LS	–	–	LS	–	–	–
	S	S	–	–	–	–	–	–
	TTL	TTL	–	–	–	–	–	–
BiCMOS	ABT	ABT	ABT	–	–	–	ABT	ABT
	ALB	–	–	–	–	–	–	–
	ALVT	–	–	–	–	ALVT	ALVT	–
	BCT	BCT	–	–	BC	–	–	BC
	LVT	LVT	LVT	–	–	–	LVT	–
CMOS	AC/ACT	AC/ACT	AC/ACT	–	AC/ACT	–	–	AC/ACT
	AHC/AHCT	VHC	–	–	VHC	–	AHC	VHC
	ALVC	VCX	ALVC	ALVC	VCX	ALVC	ALVC	VCX
	AUC	–	–	AUC	–	–	AUC	–
	AVC	–	–	–	–	AVC	AVC	–
	CBT	FST	–	FST/QS	–	PI5C	–	–
	CBTLV	–	–	CBTLV	–	PI3B	–	–
	CD4K	CD4K	–	–	MC1400	–	–	–
	FCT	–	–	FCT	–	FCT	–	–
	HC/HCT	HC/HCT	HC/HCT	–	HC/HCT	–	HC/HCT	HC/HCT
	LV-A	LVQ/LVX	LV	–	LVQ/LVX	–	LV	LVQ/LVX
	LVC	LCX	LVC	LVC/LCX	LCX	LCX/LPT	LVC	LCX

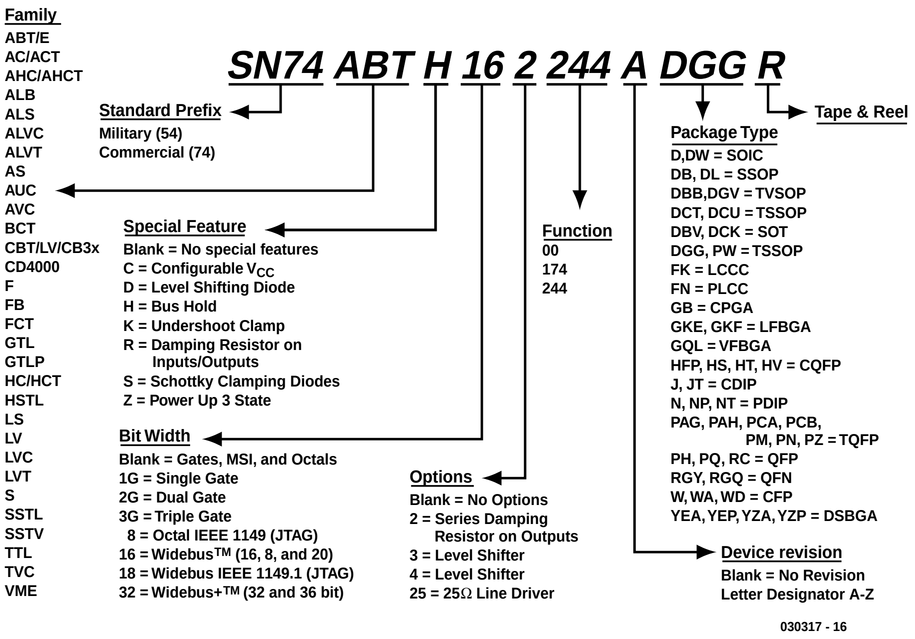


Figure 6. Texas Instruments device naming convention.

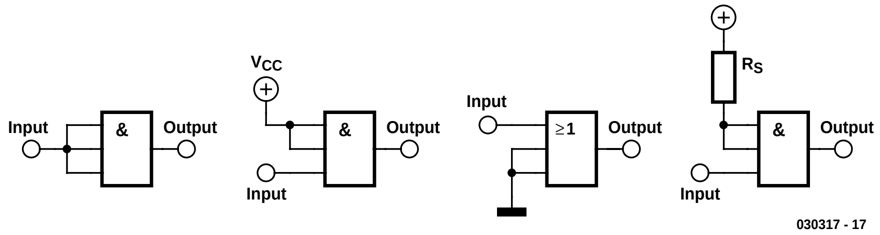


Figure 7. Do not leave unused inputs open.

Table 3. Commonly used abbreviations of manufacturer names.

AD	Analog Devices
AM	Advanced Micro Devices
AT	Atmel
bq	Benchmarq
CA	RCA (analog)
CD	RCA (digital)
CL	CComlinear Corp.
CS	Crystal Semiconductor
CS	Cherry Semiconductor
CY	Cypress Semiconductor
DG	Siliconix
DS	Dallas Semiconductor
DM	National Semiconductor (digital)
ED	IElectronic Designs Inc, EDI
EL	Elantec
EP	Altera (Classic series)
EPC	Altera (EPROM)
EPF	Altera (Flex series)
EPM	Altera (MAX series)
HA	Hitachi (analog)
HAT	Hitachi
HD	Hitachi (digital)
HI	Harris
HM	Harris Microwave
IDT	Integrated Devices Technology, IDT
IRF	International Rectifier
IP	Integrated Power
LM	National
M	Mitsubishi
MACH	Vantis (MACH, PLD)
MAX	Maxim
MB	Fujitsu
MC	Motorola
MN	Micro Networks
NDS	National Semiconductor
NE	Signetics
PI	Pericom
PM	PMI 'Analog Devices'
PWM	Siliconix
QL	Quick Logic
QSI	Quality Semiconductor
SA	Signetics
SD	SGS Thomson
SE	Signetics
SG	Silcon General
SI	Siliconix
SN	Texas Instruments, TI (Standard)
SNJ	Texas Instruments, TI (MIL/QML Qualified)
SPT	Signal Processing Technologies, SPT
SSD	Samsung Electronics
SU	Signetics
SY	Synergy Semiconductor
TA	Toshiba
TC	Toshiba
TD	Pro-Electronics
TL	Texas Instruments (analog, Linear)
TMS	Texas Instruments
X	Xicor
XC	Xilinx
XR	Exar Corp.
uA	Fairchild
UC	Unitrode integrated circuits
Z	Zilog
ZD	Zeltex

due to the risk of crosstalk.

To prevent the supply voltage from 'collapsing' when signals are switched, the inductance of the supply lines must be as small as possible, which can be achieved by measures such as using large supply and ground planes. You should also use decoupling capacitors located as close as possible to the supply pins of the ICs, in order to counter this effect. Keep current paths as short as possible in the entire circuit (for EMC!).

Never leave unused inputs open. An undefined logic level can lead to spontaneous oscillations, which can cause problems for more than just the affected gate. An oscillating gate can destroy the entire IC, or perhaps even cause the whole circuit to malfunction. Four possible solutions are shown in **Figure 7**. The simplest solution is to simply connect the unused inputs of a multiple gate together. If you use this approach, be sure to check the fan-out of the driver IC! Another solution, which does not create any fan-out problems, is to connect the unused input to one of the two logic levels, which usually means either the supply voltage or ground (shown in the middle of Figure 7). If you use TTL ICs, a series resistor (R_S) can be inserted between the supply voltage and an unused input in order to limit the current drawn by the input.

Furthermore, with flip-flops, registers and latches, you have to pay attention to set-up and hold times. Actually, that falls outside the scope of this article, but in short, what it means is that the inputs must be stable for a certain length of time before and after an active clock edge. If you want to know more, we suggest you read the data sheets and application notes from the well-known manufacturers.

Conclusion

The names of a number of well-known manufacturers, with the logic families that are currently in production and associated abbreviations, are listed in **Table 2**. A more extensive list of abbreviations, such as are found on the ICs, is given in **Table 3**.

(030317-1)